IN THE CLAIMS

Claims 14-22 and 29-37 have been withdrawn.

14. (Withdrawn) A method for determining the arrangement of contact areas of a semiconductor chip comprising:

reading semiconductor chip data, contact data and housing data;

reading production data defining the arrangement of the semiconductor chip relative to the housing;

generating an electronic device model using the semiconductor chip data, contact data, housing data, and production data; and

determining arrangement information by arranging contact areas in the electronic device model at edge regions on an active top side of the semiconductor chip, the contact areas lying on connecting lines between contact pads of the housing and an area centroid of the active top side.

15. (Withdrawn) The method of claim 14, comprising:

providing arrangement information to a fabrication process.

16. (Withdrawn) The method of claim 14, comprising:

determining a model of the active top side of the semiconductor chip; and determining electrical and logical behavior information of the semiconductor chip based on the model.

17. (Withdrawn) The method of claim 16, comprising:

determining a bonding plan based on the electrical and logical behavior information and arrangement information.

18. (Withdrawn) The method of claim 17, comprising:

providing the bonding information to a bonding machine.

19. (Withdrawn) The method of claim 14, comprising:

determining arrangement information by arranging contact areas in the electronic device model at edge regions on an active top side of the semiconductor chip, the distances between adjacent contact areas and outermost contact areas between adjoining semiconductor chip edges being formed with the same magnitude.

20. (Withdrawn) A semiconductor chip, the fabrication of which has involved performing a method as claimed in claim 14.

21. (Withdrawn) An electronic device having a housing and having a semiconductor chip arranged in or on the housing, the fabrication of the electronic device and/or of the housing and/or of the semiconductor chip having involved performing a method as claimed in claim 14.

22. (Withdrawn) A housing for a semiconductor chip, the fabrication of which has involved performing a method as claimed in claim 14.

23. (Previously Presented) A method for determining the arrangement of contact areas on an active top side of a semiconductor chip arranged in or on a housing, the method being performed on a computer system, comprising:

reading semiconductor chip data into the computer system, the semiconductor chip data comprising geometrical properties of the semiconductor chip and information about a number of contact areas to be arranged at each edge of the semiconductor chip;

reading contact area data into the computer system, the contact area data comprising geometrical and electrical properties of contact areas to be arranged on the active top side of the semiconductor chip;

reading housing data into the computer system, the housing data comprising geometrical and electrical properties of the housing and also of contact pads arranged on a top side of the housing;

reading production data into the computer system, the production data defining the arrangement of the semiconductor chip in relation to the housing;

generating a model of an electronic device, which comprises the housing and the semiconductor chip arranged with its passive rear side on the top side of the housing, from the semiconductor chip data, contact area data, housing data and production data;

arranging the contact areas in the model of the electronic device in edge regions on the active top side of the semiconductor chip; and

providing the contact area arrangement data for subsequent fabrication and/or design processes of the semiconductor chip and/or of the housing and/or of the electronic device.

24. (Previously Presented) The method of claim 23, comprising arranging the contact areas in such a way that the contact areas in each case lie on straight connecting lines between the contact pads within the housing and the area centroid of the active top side of the semiconductor chip.

25. (Previously Presented) The method of claim 23, comprising wherein in the case of contact areas arranged at a respective semiconductor chip edge, distances of identical magnitude in each case are provided between adjacent contact areas and/or between the respective outermost contact areas per semiconductor chip edge and the adjoining semiconductor chip edges.

26. (Previously Presented) The method of claim 23, comprising wherein the contact areas are firstly in each case arranged on connecting lines between the contact pads on the top side of the housing and the area centroid of the active top side of the semiconductor chip.

27. (Previously Presented) The method of claim 23, comprising wherein the contact areas arranged at an identical semiconductor chip edge are subsequently displaced such that the distances between adjacent contact areas and/or between the respective outermost contact areas

per semiconductor chip edge and the adjoining semiconductor chip edges are formed with the same magnitude in each case.

28. (Previously Presented) The method of claim 23, comprising wherein the distances between the contact areas and contact pads that are to be electrically connected to one another in each case are minimized.

29. (Withdrawn) A method for creating a bonding plan for an electronic device having a semiconductor chip and having a housing, performed on a computer system, comprising:

determining an arrangement of contact areas on an active top side of the semiconductor chip;

determining an arrangement of integrated circuits on the active top side of the semiconductor chip and/or of filler structures, which ensure an electrical connection between the contact areas and are arranged at an edge of the active top side of the semiconductor chip in each case between the contact areas;

determining a model of the active top side of the semiconductor chip, semiconductor components of the integrated circuits being defined, positioned and wired in the model at a gate level, and the model having a plurality of levels arranged above and next to one another;

checking an electrical and logical behavior of the semiconductor chip on the basis of the model using simulation and verification methods;

extracting the data required for the bonding plan from the model;

reading in housing data, which comprise geometrical and/or electrical properties of the housing and also of the contact pads arranged on the top side of the housing, into the computer system; and

creating a bonding plan on the basis of the data extracted and on the basis of the housing data, the bonding plan comprising a model of the housing and of the semiconductor chip arranged in or on the housing and also a representation of the bonding connections between the

contact areas and the contact pads.

30. (Withdrawn) The method of claim 29, comprising:

checking the bonding plan for alterations with respect to the model of the electronic device, in particular for deletions, for combinations and for interchangings of the contact areas; and

providing the bonding plan to the bonding machines.

31. (Withdrawn) The method of claim 29, wherein determining the contact arrangement comprises:

reading semiconductor chip data, contact data and housing data;

reading production data defining the arrangement of the semiconductor chip relative to the housing;

generating an electronic device model using the semiconductor chip data, contact data, housing data, and production data; and

determining arrangement information by arranging contact areas in the electronic device model at edge regions on an active top side of the semiconductor chip, the contact areas lying on connecting lines between contact pads of the housing and an area centroid of the active top side.

32. (Withdrawn) A method for generating geometry data for the creation of photomasks for the exposure of an electronic device having a semiconductor chip and having a housing by means of photolithographic methods, the method being formed on a computer system, comprising:

determining the arrangement of contact areas on the active top side of the semiconductor chip;

determining the arrangement of integrated circuits on the active top side of the semiconductor chip and/or of filler structures, which ensure the electrical connection between the contact areas and are arranged at the edge of the active top side of the semiconductor chip in

each case between the contact areas;

determining a model of the active top side of the semiconductor chip, the semiconductor components of the integrated circuits determined being defined, positioned and wired at the gate level in the model, and the model having a plurality of levels arranged above and next to one another;

checking the electrical and the logical behavior of the semiconductor chip on the basis of the model determined using simulation and verification methods; and

determining the geometry data required for the photomasks from the model of the active top side of the semiconductor chip with production tolerances being included in the calculation.

33. (Withdrawn) The method of claim 32, comprising:

checking the geometry data generated for alterations with respect to the model of the electronic device generated, in particular for displacements, for deletions, for combinations and for interchangings of the contact areas; and

providing the geometry data generated for the subsequent creation of the photomasks.

34. (Withdrawn) The method of claim 32, wherein determining the arrangement of contact areas comprises:

reading semiconductor chip data, contact data and housing data;

reading production data defining the arrangement of the semiconductor chip relative to the housing;

generating an electronic device model using the semiconductor chip data, contact data, housing data, and production data; and

determining arrangement information by arranging contact areas in the electronic device model at edge regions on an active top side of the semiconductor chip, the contact areas lying on connecting lines between contact pads of the housing and an area centroid of the active top side.

35. (Withdrawn) A computer readable medium having computer readable code for determining the arrangement of contact areas on an active top side of a semiconductor chip, comprising:

instructions for reading semiconductor chip data, contact data and housing data;

instructions for reading production data defining the arrangement of the semiconductor chip relative to the housing;

instructions for generating an electronic device model using the semiconductor chip data, contact data, housing data, and production data; and

instructions for determining arrangement information by arranging contact areas in the electronic device model at edge regions on an active top side of the semiconductor chip, the contact areas lying on connecting lines between contact pads of the housing and an area centroid of the active top side.

36. (Withdrawn) A computer readable medium having computer readable code for performing a method for creating a bonding plan for an electronic device having a semiconductor chip and having a housing, comprising:

instructions for determining an arrangement of contact areas on an active top side of the semiconductor chip;

instructions for determining an arrangement of integrated circuits on the active top side of the semiconductor chip and/or of filler structures, which ensure an electrical connection between the contact areas and are arranged at an edge of the active top side of the semiconductor chip in each case between the contact areas;

instructions for determining a model of the active top side of the semiconductor chip, semiconductor components of the integrated circuits being defined, positioned and wired in the model at a gate level, and the model having a plurality of levels arranged above and next to one another;

instructions for checking an electrical and logical behavior of the semiconductor chip on the basis of the model using simulation and verification methods;

instructions for extracting the data required for the bonding plan from the model;

instructions for reading in housing data, which comprise geometrical and/or electrical properties of the housing and also of the contact pads arranged on the top side of the housing, into the computer system;

instructions for creating a bonding plan on the basis of the data extracted and on the basis of the housing data, the bonding plan comprising a model of the housing and of the semiconductor chip arranged in or on the housing and also a representation of the bonding connections between the contact areas and the contact pads.

37. (Withdrawn) A computer readable medium having computer readable code for performing a method for generating geometry data for the creation of photomasks for the exposure of an electronic device having a semiconductor chip and having a housing by means of photolithographic methods, comprising:

instructions for determining the arrangement of contact areas on the active top side of the semiconductor chip;

instructions for determining the arrangement of integrated circuits on the active top side of the semiconductor chip and/or of filler structures, which ensure the electrical connection between the contact areas and are arranged at the edge of the active top side of the semiconductor chip in each case between the contact areas;

instructions for determining a model of the active top side of the semiconductor chip, the semiconductor components of the integrated circuits determined being defined, positioned and wired at the gate level in the model, and the model having a plurality of levels arranged above and next to one another;

instructions for checking the electrical and the logical behavior of the semiconductor chip on the basis of the model determined using simulation and verification methods; and

instructions for determining the geometry data required for the photomasks from the model of the active top side of the semiconductor chip with production tolerances being included in the calculation.